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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/029,979	12/31/2001	Toshio Miyamoto		6075

7590 01/16/2004

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EXAMINER	
CHAMBLISS, ALONZO	
ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 01/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/029,979	MIYAMOTO ET AL.	
	Examiner	Art Unit	
	Alonzo Chambliss	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 October 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *49-74* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *49-74* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *8* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Amendment C filed on 10/27/03 has been fully considered and made of record in Paper No. 9.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 49-74, insofar as definite, are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyazaki (U.S. 6,342,726) in view of Carpenter (U.S. 5,541,448)

With the respect Claims 49, 57, 58, 62, 63, and 74, Miyazaki discloses providing first semiconductor devices 13 each having a DRAM semiconductor chip and protruded terminals arranged over the DRAM semiconductor chip. A second semiconductor

device has a package body, a nonvolatile memory semiconductor chip (i.e. DRAM) sealed in the package body and outer leads protruding outwardly from a side surface of the package body. The first and second devices are DRAM devices that are configured as a chip scale package and a QFP. Miyazaki discloses wherein each of the first semiconductor devices is a DRAM device, which is a nonvolatile read-only memory device (see col. 12 lines 15-18). It is well known in the semiconductor industry to interchange DRAMs devices with EEPROM devices (i.e. read-only memory) as evidence by Carpenter (see col. 1 lines 17-24). Therefore, it would have been obvious to one skilled in the art at the time of the invention to interchange an EEPROM for the second device of Miyazaki, since the EEPROM is a nonvolatile memory device provides a stable memory device for the integrated circuit card as taught by Carpenter. A module board having first terminals and second terminals; and mounting the first semiconductor devices 13 and the second semiconductor device 14 on the module board, wherein the mounting step is performed such that the protruded terminals of the first semiconductor devices 13 are arranged between the DRAM semiconductor chips of the first semiconductor devices and the module board 15 in a sectional view and arranged at the inside of the DRAM semiconductor chips of the first semiconductor devices in a plan view, and the protruded terminals of each of the first semiconductor devices are soldered to the first terminals of the module board 15 and such that the outer leads of the second semiconductor device are soldered to the second terminals of the module board 15 at the outside of the package body in the plan view (see col. 12 lines 5-30; Figs. 1-4).

With respect to Claims 50 and 64, Miyazaki discloses wherein in the mounting step, the protruded terminals are arranged in rows and columns between each of the DRAM semiconductor chips 13 of the first semiconductor devices and the module board (see Figs. 3 and 4).

With respect to Claims 51 and 65, Miyazaki discloses wherein each of the outer leads of the second semiconductor device 14 is exposed to the air between the package body and a portion of the outer leads that connect to the second terminals (see Figs. 3 and 4).

With respect to Claims 52 and 66, Miyazaki discloses wherein each of the DRAM semiconductor chips 13 of the first semiconductor devices has a main surface and bonding electrodes on the main surface, and wherein the protruded terminals are arranged over the main surface and electrically connected to the bonding electrodes (see Figs. 3 and 4).

With respect to Claims 53 and 67, Miyazaki discloses wherein the mounting step is performed so that the main surfaces of the DRAM semiconductor chips of the first semiconductor devices face the module board (see Figs. 3 and 4).

With respect to Claims 54 and 68, Miyazaki discloses wherein in surface of the DRAM semiconductor the mounting step, back chip of each of the first semiconductor devices are exposed (see Figs. 3 and 4).

With respect to Claims 55 and 69, Miyazaki discloses sealing a space (i.e. a portion between the active surface of chip 1 to the upper surface of solder resist 4) that

is between each of the first semiconductor devices 13 and the module board 15 with resin 6 (see col. 11 lines 10-27; Figs. 1 and 2).

With respect to Claims 56 and 70, Miyazaki discloses wherein all protruded terminals of each of the first semiconductor devices are arranged between the corresponding semiconductor chip of the corresponding first semiconductor device and the module board (see Figs. 3 and 4).

With respect to Claims 59 and 71, one skilled in the art would readily recognize to simultaneously soldering the first semiconductor devices and the second semiconductor device to mount them on the module board after the step of arranging the first semiconductor devices and the second semiconductor device on the module board after the step of arranging the first and second devices, since simultaneously soldering a plurality of devices would save time during manufacturing which would reduce the cost of the memory module. Therefore, it would have been obvious to incorporate the simultaneous soldering of the first and second devices of Miyazaki, since simultaneously soldering a plurality of devices would save time during manufacturing which would reduce the cost of the memory module.

With respect to Claims 60 and 72, Miyazaki discloses wherein an umber of the first semiconductor devices 13 is larger than that of the second semiconductor device 14 on the module board 15 (see Fig. 4).

With respect to Claims 61 and 73, Miyazaki discloses wiring portions 10,11 for expanding the pitch of the protruded terminals 5 to be wider than the pitch of the

bonding electrodes 7 of semiconductor chip 1 in the first semiconductor devices 13 (see Figs. 1 and 2).

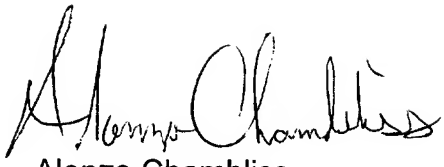
Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning the communication or earlier communications from the examiner should be directed to Alonzo Chambliss whose telephone number is (703) 306-9143. The fax phone number for this Group is (703) 308-7722 or 7724.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-7956



Alonzo Chambliss
Patent Examiner
Art Unit 2827

AC/January 12, 2004